Abstract of the Disclosure

The present invention relates to a device for an interrupt verification support mechanism and the method for operating said device comprising a processor and an input for external interrupt requests or interrupt pseudo-instructions communicatively coupled to the processor. The method comprises the steps of processing at least one actual instruction in the processor in an instruction pipeline, and if an external interrupt request is received by the processor, the actual instruction is replaced with the pseudo-instruction. Pursuant to the method, instructions are concurrently processed in the processor in an instruction pipeline with several stages. In the instruction pipeline, instructions are processed by an instruction fetch stage, an instruction decode stage, an instruction issue stage, an execute stage and a result write-back stage. Thereby, interrupt requests are only processed at the fetch stage of the instruction pipeline. The device of an interrupt support mechanism and the method for operating said device provides the advantage a simplification of interrupt verification.